REMARKS

Claims 1-19 are presented for examination. Claim 8 is found allowable subject to being rewritten in independent form.

The Examiner has withdrawn all rejections raised in the previous Office Action. Rejections based on new grounds have been raised.

In particular, claims 1-4, 7- 9-15, 17 and 19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuroda et al. in view of Bando et al. (newly applied reference). Dependent claims 5, 6, 16 and 18 have been rejected under 35 U.S.C. § 103 as being unpatentable over Kuroda and Bando et al in view of Bowen et al.

It is noted that the Examiner did not provide a Notice of References Cited (PTO-892) with the newly applied Bando et al. reference.

The rejections are respectfully traversed for the following reasons.

Claim 1 recites a memory system for a portable telephone including a signal transmission/reception portion for transmitting and receiving a signal and a control portion for controlling at least a signal transmission and reception operation of said transmission/reception portion.

The memory system comprises:

- a random access memory providing a working area for said control portion; and

- a flash memory including a memory array for storing a program for said control portion and at least transmission and reception data in a non-volatile manner under a control of said control portion.

Claim 1 specifies that the memory array is divided into a plurality of storage units, and a register, provided commonly to the respective storage units, and having information in a storage unit of said plurality of storage units transmitted thereinto for temporal storage of the transmitted information and allowing serial readout of the transmitted and stored information.

Further, independent claim 12 also recites that the memory array is divided into a plurality of storage units. The claim specifies that a plurality of pieces of information in one unit of the storage units selected in accordance with an address signal at a time, are allowed to be serially read out in synchronization with a clock signal without further address application.

First, it is respectfully submitted that the Examiner has failed to address this limitation of claim 12. However, neither of the applied references teaches or suggests the claimed arrangement.

Further, the Examiner takes the position that Kuroda differs from the arrangement claimed in claim 1 only in that the reference does not disclose "temporal storage of the transmitted information." The Examiner relies upon Bando for disclosing "downloading a program which is temporarily stored in the temporal storage area {p. 3 [0058]}."

In particular, the Examiner considers that the Kuroda teaching of reading data onto the common data line implements the serial operation recited in claim 1, and maintains that the data reading onto the common data line suggests the claimed register.

This position is respectfully traversed. Kuroda discloses that data is read out from a selected memory cell in the memory cell array onto the common data line and then transferred through the sense amplifier for each data bit.

In particular, in the arrangement of Fig. 13 of Kuroda, the common data line is provided corresponding to each memory cell array, and is not provided commonly to a plurality of memory blocks or memory cell arrays (storage units).

According to the arrangement of Fig. 35 of Kuroda, each memory array ARY is divided into a plurality of memory blocks LMB and 8MB by word lines, and a memory cell is selected in either of memory block and is coupled to the common data line.

Claim 1 requires the register to allow serial readout of the transmitted and stored information.

By contrast, in Kuroda, an address is supplied for each access cycle and data is read out. The operation mode in which data is supplied in synchronization with the clock signal is the data writing mode, and the programming is performed when data of 4-byte length is stored in the input latch DIL, which is employed only in the data writing mode to sequentially store the data of a byte length applied serially in synchronization with the clock signal. Writing of data is performed in 4-byte units. One skilled in the art would understand from the reference that the writing indicates the writing of "1" and "0" and the programming indicates the operation of

writing of "I" or electron injection into the floating gate of the memory cell transistor. Therefore, the input latch of Kuroda implements the serial/parallel conversion in data writing and does not perform the serial readout operation.

Fig. 26 of Kuroda shows an output latch DOLA provided for switching the data bit width between 8 bits and 16 bits. In reading of 16-bit data, the output latch DOLA stores 80-bit data sequentially to output 16-bit data, and implements the serial/parallel conversion function. Thus, output latch DOLA of Kuroda does not allow serial readout of data transmitted from the selected memory cells.

Hence, Kuroda does not disclose the claimed register, provided commonly to the respective storage units, and allowing serial readout of the transmitted and stored information.

Further, as discussed above, the Examiner admits that Kuroda does not disclose "temporal storage of the transmitted information." She relies upon Bando for disclosing "downloading a program which is temporarily stored in the temporal storage area {p. 3 [0058]}."

Considering Bando, the reference discloses the arrangement in which program storage regions 48 and 49 and a temporal storage region 50 are provided in a flash memory. Upon loading of downloaded program, the downloaded program is once stored in the temporal storage region and then is subject to the interpreter process such as a decision of normal/failure of the program. After the interpreter processing, the program is stored in the program storage region.

Bando does not disclose the program information transferred between the storage regions.

The Examiner considers the temporal storage as the claimed register. However, the temporal storage of Bando is employed for storing the externally downloaded program prior to storage of the program in the program storage region and the verification of erasure of a program in the program storage region. Thus, Bando does not disclose storing the program information read out from the program storage region into the temporal storage region for further transfer.

Hence, Bando does not teach or suggest the claimed register, provided commonly to the respective storage units, and having information in a storage unit of said plurality of storage units transmitted thereinto for temporal storage of the transmitted information, as claim 1 requires.

Moreover, it is incumbent upon the Examiner to provide a basis in fact and/or cogent technical reasoning to support the conclusion that one having ordinary skill in the art would have been motivated to combine references to arrive at a claimed invention. ***Uniroyal, Inc. v. Rudkin-Wiley Corp.***, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). The Examiner offered no logical reason, and no such reason is apparent, to support the conclusion that one having ordinary skill in the art would have been impelled to combine Bando with Kuroda.

In particular, the Examiner has taken the position that it would have been obvious "to modify Kuroda to include temporal storage for the purpose of executing interpreter processing in a program rewrite control section."

It is noted that the Examiner considers the memory sections ARY0-ARY7 (FIGS. 13 and 35 of Kuroda) to correspond to the plurality of storage units. The data line CD is considered to correspond to the claimed register.

It is respectfully submitted that one skilled in the art would find nor reason to modify the data line CD of Kuroda "to include temporal storage for the purpose of executing interpreter processing in a program rewrite control section." Moreover, one skilled in the art would realize that Kuroda does not need to execute "interpreter processing."

Further, as demonstrated above, neither Kuroda nor Bando discloses the claimed register, provided commonly to the respective storage units, and allowing serial readout of the transmitted and stored information.

Moreover, neither Kuroda nor Bando discloses that the claimed register has information transmitted thereinto for temporal storage.

Accordingly, even if Kuroda were modified as the Examiner suggests, the claimed arrangements would not result.

In particular, combined teachings of the references would not teach or suggest that information in a storage unit of the plurality of storage units is transmitted into the data line CD of Kuroda for temporal storage of the transmitted information, and that the data line CD allows serial readout of the transmitted and stored information, as claim 1, requires.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As demonstrated above, the prior art teachings are not sufficient to arrive at the invention recited in claim 1.

Further, claim 12 requires the one-time application of an address for selecting information of multi bits, and serial readout of the bits of the selected information without further application of an address.

Neither Kuroda nor Banda discloses that a plurality of pieces of information in one unit of the storage units selected in accordance with an address signal at a time, are allowed to be serially read out in synchronization with a clock signal without further address application, as claim 12 recites.

Therefore, the combined teachings of these references are not sufficient to suggest the arrangement recited in claim 12.

Dependent claims 2-7, 9-11, and 13-19 are defined over the prior art at least for the reasons presented above.

Accordingly, the Examiner's conclusion of obviousness with respect to claims 1-7, and 9-19 is unwarranted. Therefore, the rejections of these claims under 35 U.S.C. 103 are improper and should be withdrawn.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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